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AD9144-EBZ Evaluation Board Quick Start Guide

Getting Started with the AD9144-EBZ Evaluation Board and Software

What's in the Box

- AD9144-EBZ Evaluation Board (Rev 2 Silicon)
- Evaluation Board CD
- Mini-USB Cable

Recommended Equipment List

- +5Vdc, Power Supply
- 2 Sinusoidal Clock Sources
- Spectrum Analyzer
- Data Pattern Generator Series 3 (DPG3)

Introduction

The AD9144-EBZ connects to a DPG3 for quick evaluation of the AD9144, a high-speed, signal processing Digital to Analog Converter. The DPG3 automatically formats the data and sends it to the AD9144-EBZ, simplifying evaluation of the device. The Evaluation Board (EVB) runs from a +5V supply. A clock distribution chip AD9516 is included on this EVB as a clock fan-out and frequency divider for the DACCLK, REFCLK and DPG3 input clock. Figure 2 is an image of the top side of the AD9144-EBZ.

AD9144 Evaluation Software

The AD9144 Evaluation Board software has an easy-to-use graphical user interface (GUI). It is included on the Evaluation Board CD, or can be downloaded from the DPG website at

http://www.analog.com/dpg. This will install DPGDownloader (for generating and loading vectors into the DPG3) and AD9144 SPI software.

Hardware Setup

Connect +5.0V to P5, GND to P6. A low phase noise high frequency clock source should be connected to the SMA connector, J1. This is the DACCLK input. The spectrum analyzer should be connected to the SMA connector, J4. A +1.0V power supply must be connected to the VTT probe point near SMA connector J9, along with a GND connection to the GND probe point next to it. The evaluation board connects to the DPG3 through the connectors P4. The PC should be connected to the EVB using the mini-USB connector XP2 after installation of the Evaluation Board software. Figure 1 shows the block diagram of the set-up.

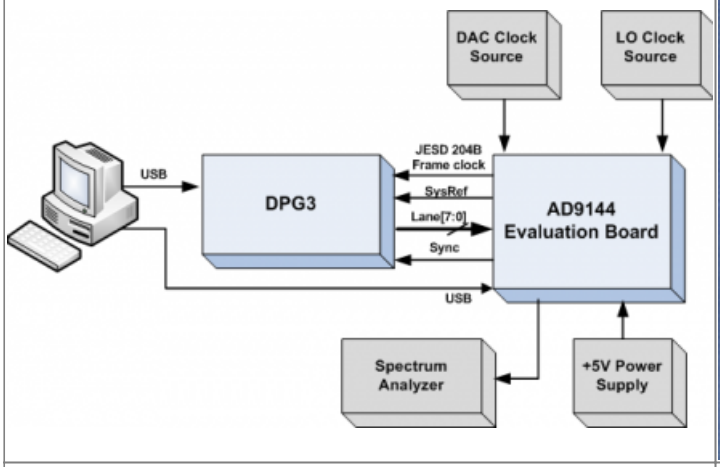

Figure 1. Block diagram of the AD9144 lab bench set-up

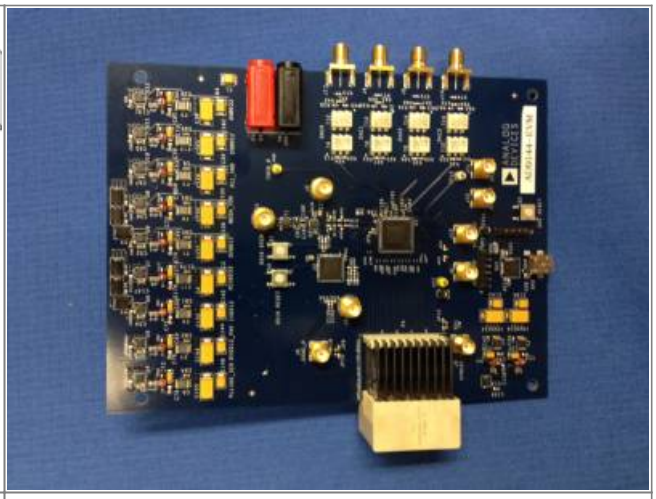

Figure 2. Top view of AD9144-EBZ

Getting Started

The PC software comes on the included Evaluation Board CD, but may also be downloaded from the DPG Web site at http://www.analog.com/dpg. The installation will include the DPG Downloader software as well as all the necessary AD9144 files including schematic, board layout, datasheet, AD9144 SPI, and other files.

Initial Set-Up

1. Install the DPG Downloader and AD9144 SPI software and support files on your PC. Follow the instructions in the installation wizard and use the default (recommended) installation settings.

2. Use a USB cable to connect the EVB to your PC and connect the lab equipment to the EVB.

3. Connect the DGP3 unit to your PC and turn on the unit.

Single-Tone Test using DAC PLL

These settings configure the AD9144 to output a sine wave using the DPG3 and allow the user to view the single-tone performance at the DAC output, under the condition: Fdata = 368.64MHz, 4X interpolation, IF = 20MHz.

Configure DPG Vector Software

1. To begin, turn on the external +5V supply 2. Open DPG Downloader if you have not done so. (Start > All Programs > Analog Devices > DPG > DPGDownloader). Ensure that the program detects the AD9144, as indicated in the “Evaluation Board” drop-down list as “JESD204”, and select it. The “Data Clock Frequency” window will show (0 or 19 MHz)because the SPI software had not been started. The DPG Downloader panel should look like Figure 3.

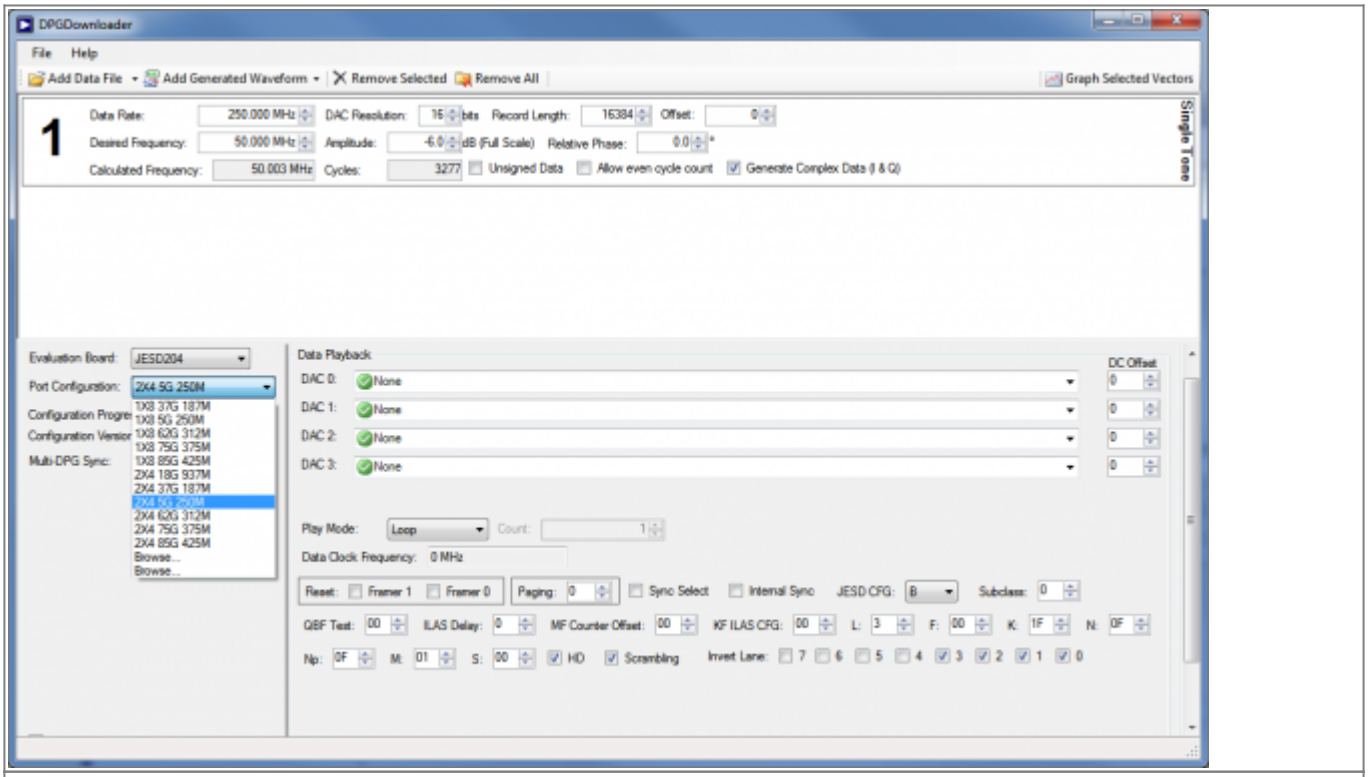

Figure 3. DPG Downloader Panel

3. Click on “Add Generated Waveform”, and then “Single Tone”. As shown in Figure 4, a Single Tone panel will be added to the vector list. Enter the sample rate, in this case 250MHz and the desired frequency, 50MHz. Enter the digital amplitude. In this case we use -6dBFS. Check the “Generate Complex Data (I & Q)” box and uncheck the “Unsigned Data” box. Select the In-Phase data vector in the “DAC0” and “DAC2” drop down menu and the Quadrature data vector in the “DAC1” and “DAC3”.

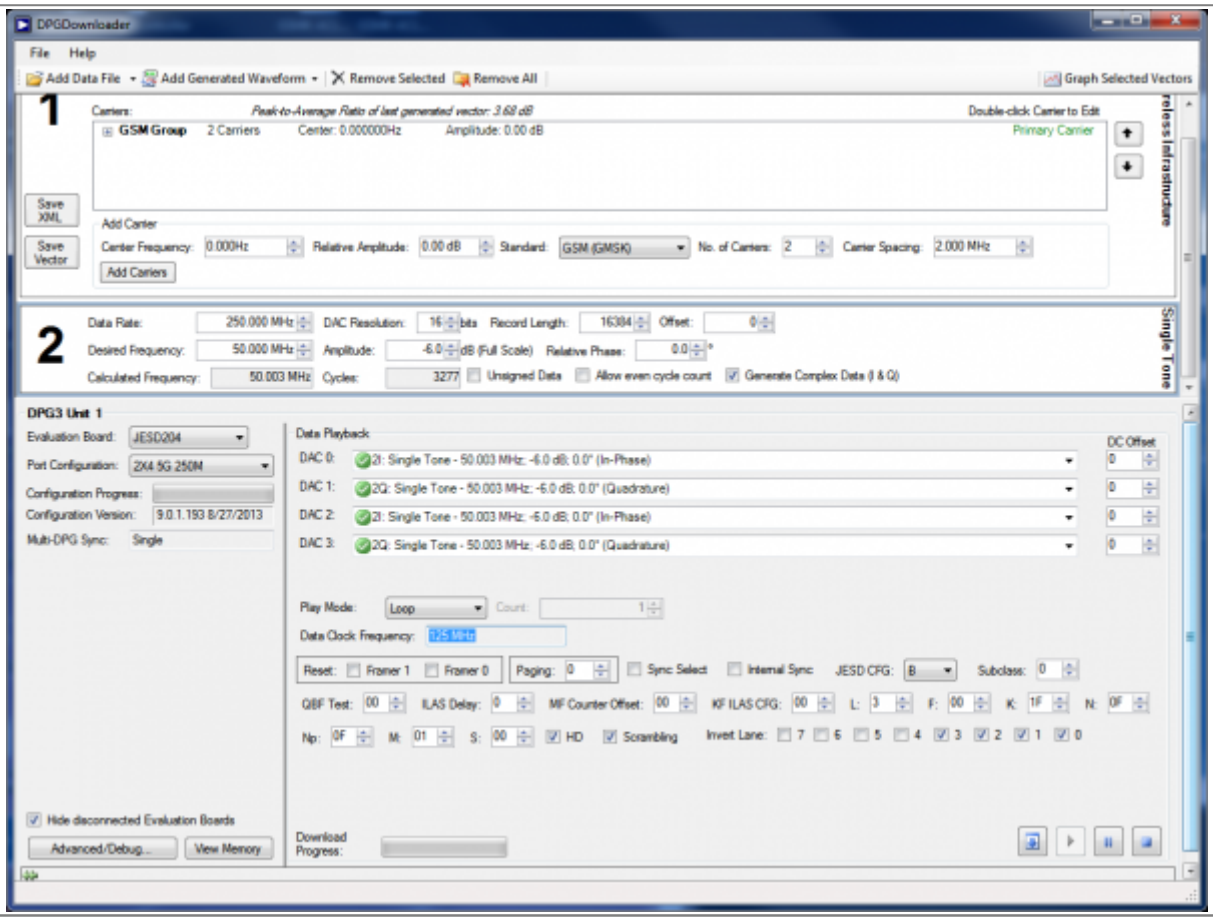

Figure 4. DPG Downloader sinewave vector

Configuring SPI

1. Open the AD9144 SPI application (Start > All Programs > Analog Devices > AD9144 > AD9144 SPI). The screen should look similar to Figure 5.

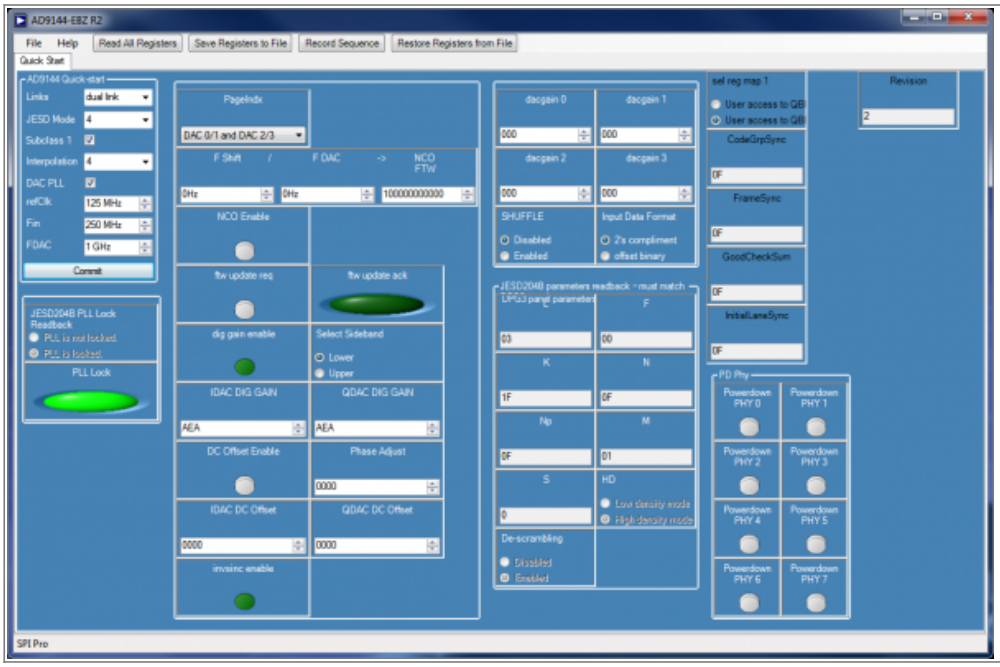

Figure 5. Entry Screen of the AD9144 SPI software

2. Configure the hardware according to the hardware set-up instructions given in the Hardware Setup section above. Set the frequency of the DAC clock signal generator to 250MHz, and the output level to 3dBm. The spectrum analyzer can be configured with Center Frequency = 200 MHz, Span = 400 MHz, and Resolution Bandwidth of 30 kHz. Choose Input Attenuation to be 20dB. This can be adjusted later if indications are that the analyzer is causing degradations.

3. Follow the sequence below to configure the AD9144 SPI registers.

a. Open the AD9144 customer SPI software and go to the Quick Start tab (See Figure 5). The parameters in top left corner need to be selected in the Quick Start List shown in the panel below. The Links should be set to dual link, mode which is interface mode set to 4, Subclass 1 box checked, Interpolation set to 4, the DAC PLL box checked,refCLK = 125MHz, Fin =250Mhz and FDAC set to 1000 MHz.

b. Click “Commit” button to initialize the AD9144. At this point both the JESD204B PLL should be locked and the DAC PLL should locked indicated with bright green PLL button.

c. Click “Read All Registers” in the top menu bar.

d. Make sure the JESD204B parameters in the DPG Downloader panel match what’s shown in the “JESD204B parameters readback” in the AD9144 SPI software. If not, change the ones in the DPG Downloader panel.The four registers “codeGrpSync, FrameSync, GoodCheckSum and Initial LaneSync” should all read 0F indicating the lanes are working correctly. If you are using a different interface mode than 4 these register will read different codes. At this point the data clock frequency on the LED panel of the DPG3 and in the DPG3 software panel should read ½ the Data rate frequency 125MHz.

e. Click Download () and Play () in the DPG Downloader screen.

f. Click “Read All Registers” in the top menu bar. You should see “JESD204B PLL Lock Readback” shows “PLL is locked”.

g. The current on the 5V supply should read about 1600mA. If you do not see the output, gently push the board toward the DPG3. This ensures that the board is firmly connected to the DPG3. The four registers codeGrpSync, FrameSync, GoodCheckSum and Initial LaneSync should all read 0F indicating the lanes are working correctly. At this point the data clock frequency on the LED panel of the DPG3 and in the DPG3 software panel should read ½ the Data rate frequency 125MHz.

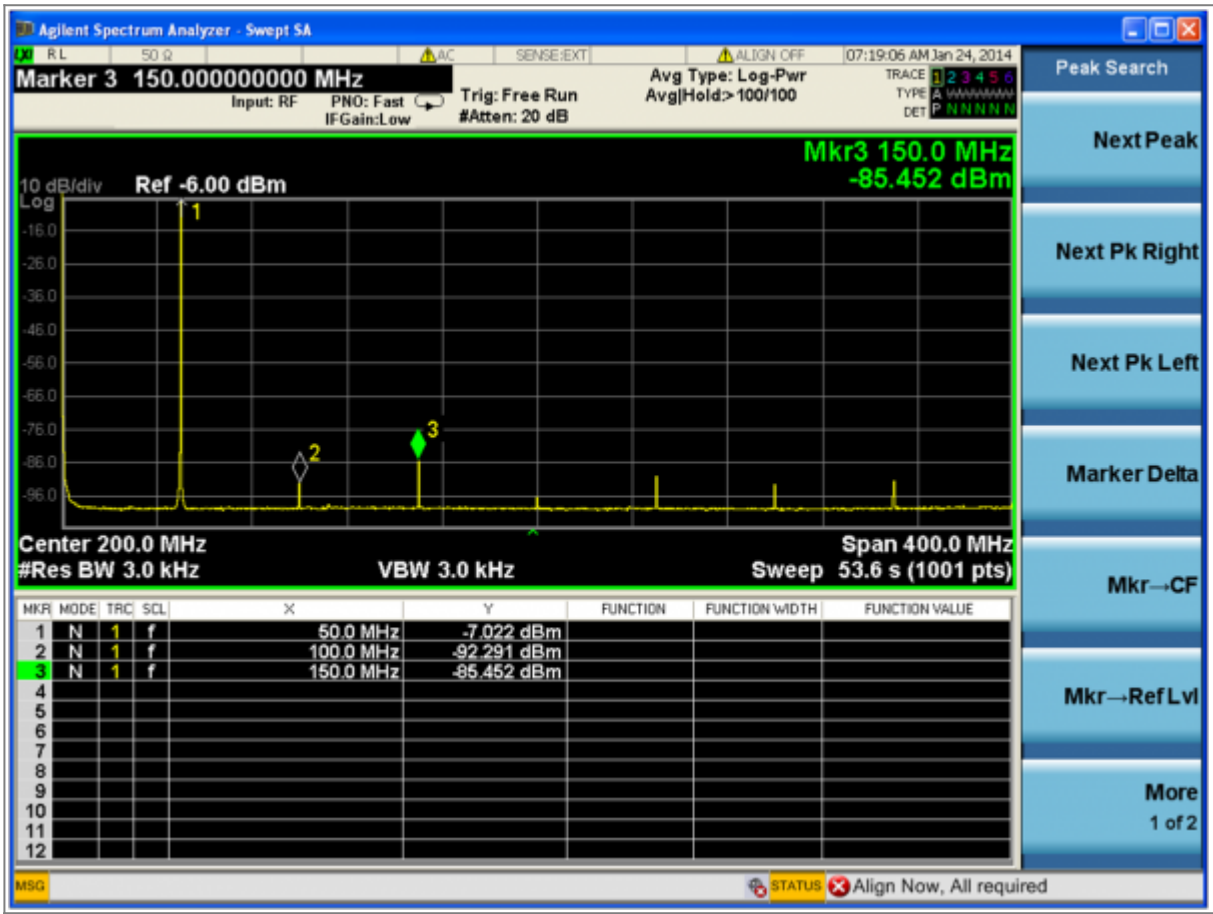

Figure 6. AD9144-EBZ Eval Board output Spectrum

ConfSingle Tone using the NCO

1. The NCO is used by loading the FDAC to 1GHz and selecting the shift frequency, for this example we will use 75MHz. The click the NCO Enable button, the NOC FTW will change from 00000 to 13333333.xt click the ftw undate req button, the ftw update light should turn bring green at this pointSee Figure 7

2. The DAC outputs will shift up to 125MHz (Sum on input and the NCO freq shift) See Figure 8.

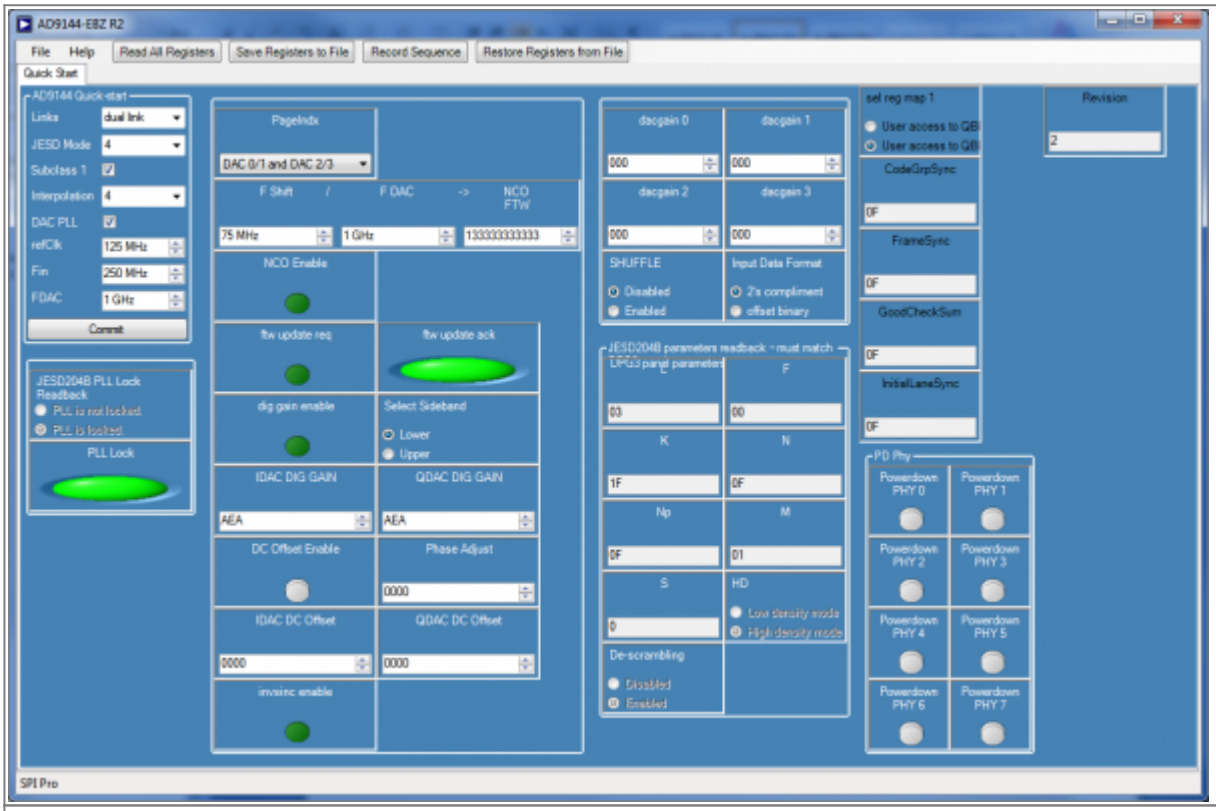

Figure 7. SPI Setting for using NCO

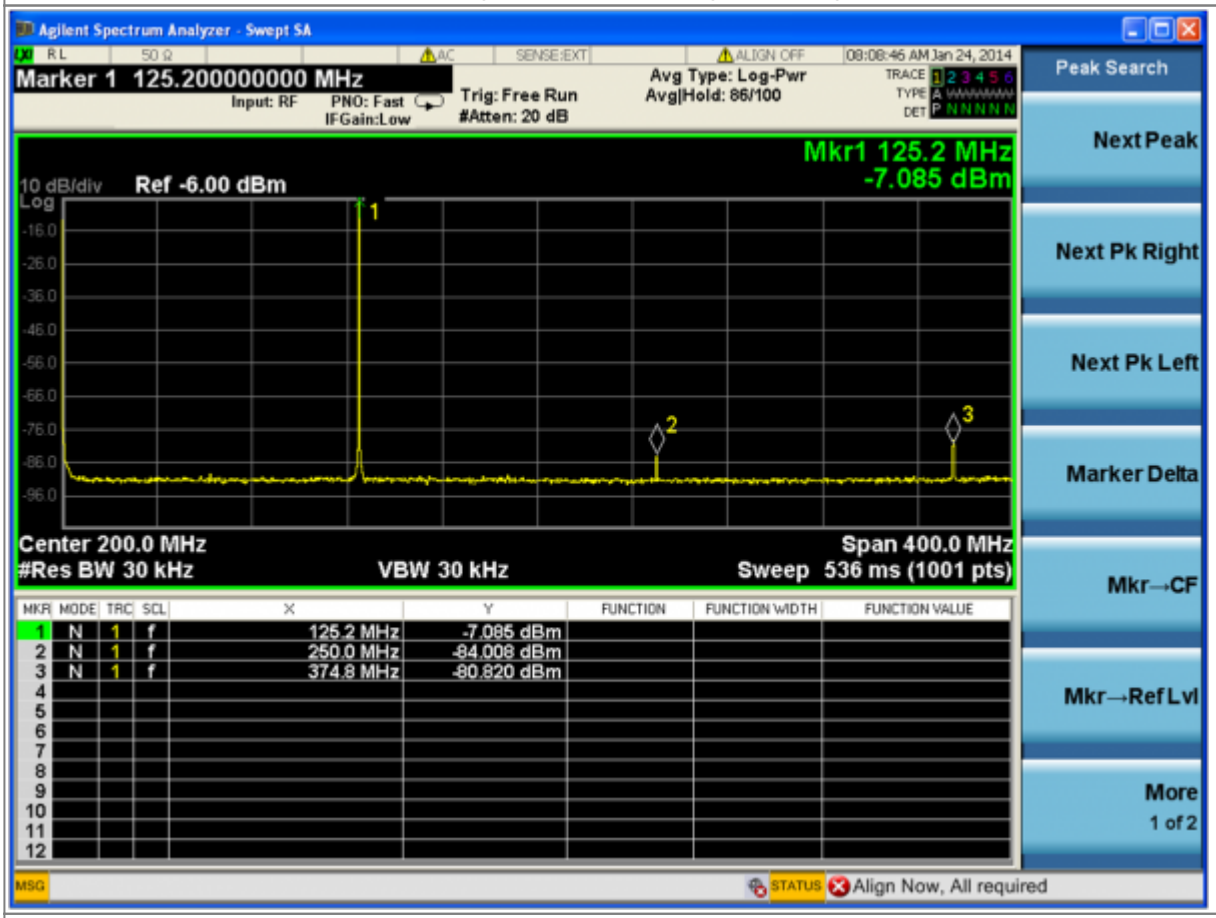

Figure 8. SPI Setting for using NCO